REMARKS

The present response is intended to be fully responsive to all points of rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Claims 1-34 are pending in this case. Claims 1-4, 6-7, 10-13, 16-17, 19, 26-31, 33-34 have been rejected under 35 U.S.C. § 103(a). Claims 5, 8-9, 14-15, 18, 20-25, 32 have been objected to. Independent claims 1, 6, 16 and 28 have been amended.

With respect to the Examiner's 35 U.S.C. § 103(a) rejections, Applicant has reviewed the cited art and respectfully submits that the art fails to disclose or suggest the Applicant's claimed invention. Therefore, Applicant respectfully traverses and requests favorable reconsideration.

Telephonic Interview

Applicant wishes to thank the Examiner for granting a telephone interview on November 9, 2005. The interview participants included Examiner Jaison Joseph and Howard Zaretsky (Applicant's representative).

Response to 35 U.S.C. § 103(a) Rejections

Regarding claims 1-4, 19:

The Examiner rejected claims 1-4, 19 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,813,262 ("Lee et al.") in view of U.S. Patent No. 6,650,689 ("Oishi et al.") and further in view of U.S. Patent No. 6,173,008 ("Lee").

While continuing to traverse the Examiner's rejections, Applicant, in order to expedite the prosecution, has chosen to clarify and emphasize the crucial distinctions between the present invention and the devices of the patents cited by the Examiner. Specifically, claim 1 has been amended to include a correlator for correlating an input **data** signal with a code, **for use in effectively realizing a plurality of rake receiver fingers** comprising a sample register adapted to store and output E input data samples every chip period of an input sample stream clocked at an over sampling ratio of R times a nominal sampling clock rate, a single code register adapted to store and output a code value at the nominal sampling clock rate, a single multiplier coupled to the sample register and the code register, the multiplier adapted to multiply the output of the sample register with the output of the code register, a single adder adapted to add the output of the multiplier with a correlation sum output of the last stage of an M-stage integration result shift register and to produce an updated correlation sum therefrom, the integration results shift register adapted to store M

correlation sums wherein updated correlation sums output of the adder are shifted into the integration results shift register at the over-sampling clock rate such that the over-sampling phase of the correlation sum at the output of the integration results shift register corresponds to the correlation sum currently at the input to the adder and wherein E, R and M are positive integers.

Lee et al. teaches a synchronization tracking device and method in a code division multiple access (CDMA) receiver including oversampling received signals corresponding to a plurality of chips at a predetermined speed and sequentially storing the oversampled signals in a received signal shift register unit. The pseudo noise codes generated in a pseudo noise code generator are sequentially stored in a pseudo noise code shift register unit in a chip unit. The output data from the received signal shift register unit is correspondingly multiplied with the pseudo noise codes output from the pseudo noise code shift register unit by means of a plurality of multipliers. The data outputted from the plurality of multipliers is added and stored as the phase information and energy value for one path. The above procedure is repeatedly performed until the phase information and energy values for all paths are stored. The path corresponding to a largest value in the stored phase information and energy values for all paths is selected and a demodulator is informed of the selected path. Thereby, the synchronization tracking device can reduce the time necessary for the synchronization tracking and continuously correct the information for a selected path, thereby improving the performance of the receiver.

The correlator of Lee et al. is operative to simultaneously perform a plurality of multiply operations and to sum their results. This is achieved using the bank of multipliers 700, thus greatly increasing the hardware requirements of this correlator.

In contrast, the present invention utilizes a single multiplier and adder to sequentially perform correlation operations sequentially. In operation, the input data samples are multiplied with the code and the results are accumulated in the integration results shift register. This feature is neither taught nor suggested by Lee et al.

Oishi et al. teaches a correlator that reduces the scale of circuitry and shortens the code phase detection time needed to achieve initial synchronization. In a correlator for calculating correlation between a received spreading code contained in a received spread-spectrum signal and a reference spreading code, a combined code generator is included. The combined code generator outputs a combined spreading code by weighting and combining a plurality of phase-shifted reference spreading codes A_1 - A_M. Further, an arithmetic circuit calculates correlation between the received spreading code and the plurality of phase-shifted reference spreading codes simultaneously. A phase detection circuit detects the phase difference between the received spreading code and a reference

spreading code, namely the phase of the received spreading code from the results of the arithmetic operation.

Oishi et al. is operative to correlate two PN codes whereby one of the PN codes is delayed and each tap is weighted. The resultant plurality of weighted taps are combined and correlated with a received spreading code.

In contrast, the present invention is adapted to perform the correlation of in put data samples with one or more codes thereby effectively realizing multiple fingers using a single multiplier and adder. This feature is neither taught nor suggested by Oishi et al.

Lee teaches a rake receiver for receiving a data signal transmitted from a transmitter in a spread spectrum communication system. The rake receiver includes a symbol combiner having an adder for adding Walsh index output values, sequentially generated from a correlator using a fast Walsh transform algorithm according to N Walsh code sequences, to a value generated from a last stage of an N-stage shift register, and having the N-stage shift register for shifting an accumulated value of an output of a rake receiver corresponding to each index for a Walsh symbol generated from the adder each time a rake is assigned to each finger. The rake receiver also includes a first decision logic unit for determining a maximum value by sequentially sorting an output of the symbol combiner and generating a Walsh index corresponding to the determined maximum value as a code word; and a second decision logic unit for sorting and subtracting the output of the symbol combiner according to a state of each bit of a corresponding index and generating a probability value for the code word.

Lee teaches using multiple multipliers (36-1 through 36-N, Figure 2) to implement the correlator in a rake receiver. The input is multiplied by complex weights by the correlator. The single correlator simultaneously correlates the samples with several code sequences using an FWT algorithm. The correlation results are then multiplied by complex weights in the multipliers 36-1 to 36-N (Figure 2). Further processing of the output of the multipliers are further processed and applied to a shift register. Each of the registers of the shift register includes the accumulated value of the rake receiver output corresponding to each index of a Walsh symbol. Each register output is input to hard and soft decision logic. This solution, however, is hardware intensive as it requires N multipliers to simultaneously perform N multiplications.

In contrast, the correlator of the present invention uses a single multiplier and a single adder to effectively realize a plurality of fingers in a rake receiver. Only a single multiplier and adder are required since they are shared sequentially (i.e. multiplexed) for each finger realized. This feature is neither taught nor suggested by Lee.

It is submitted that the present invention is a reduced complexity correlator wherein a single multiplier and adder operate in conjunction with an integration results shift register. The integration results shift register is adapted to store a plurality of partial correlation sums, one for each input sample/code combination. The correlation sums are calculated over multitude symbol times wherein a correlation sum is maintained for each sample time within the symbol and for each code (in the case of multiple codes per sample). In operation, the clocking of the sample register, code register and integration results shift register is adjusted such that the correlation sum output of the integration results shift register corresponds to the correlation result presently being calculated. A feature common to all the embodiments is the use of a **single** multiplier and a **single** adder regardless of the number of input data samples and codes to be correlated. **This permits the most complex parts of the correlator (i.e. the multiplier and adder) to be reused. Thus, the invention is able to achieve significantly lower gate counts in realizing rake receiver fingers in a spread spectrum receiver.** These features are neither taught nor suggested by the Lee et al., Oishi et al. or Lee references.

It is submitted that the combination of Lee et al., Oishi et al. and Lee would not result in the claimed invention. The combination suggested by the Examiner fails to teach or suggest all the limitations of each claim. The combination of Lee et al., Oishi et al. and Lee fails to teach a single multiplier, single adder and integration results shift register as taught by the present invention.

The Applicant respectfully traverses the rejection of claims 1-4, 19 and submits that the presently claimed invention are patently distinct over Lee et al. in new of Oishi et al. and further in view of Lee. It is believed that claims 1-4, 19 overcome the Examiner's § 103(a) rejection based on the Lee et al., Oishi et al. and Lee references. The Examiner is respectfully requested to withdraw the rejection based on § 103(a).

Regarding claims 6-7, 10-13, 16-17, 19, 28, 31:

The Examiner rejected claims 6-7, 10-13, 16-17, 19, 28, 31 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,813,262 ("Lee et al.") in view of U.S. Patent No. 6,650,689 ("Oishi et al.") and U.S. Patent No. 6,173,008 ("Lee") and further in view of U.S. Patent No. 6,539,048 ("Hakala").

Hakala teaches a mobile station for receiving a spread spectrum, code division transmission from at least one transmitter, such as a base station. The mobile station contains a receiver for outputting data samples, and further contains a multi-tap ring matched filter. The ring matched filter is constructed to have first circuitry for storing an individual one of a received data sample into an

individual one of a plurality storage registers such that an active data sample that has been stored for the longest period of time is overwritten with a most recently received data sample. The ring matched filter is further constructed to have second circuitry for serially shifting coefficient bits of at least one multi-bit spreading code relative to the storage registers for sequentially and simultaneously correlating the at least one multi-bit spreading code with a plurality of corresponding stored data samples, while significantly reducing power consumption by limiting state changes of flip-flops.

For the reasons stated hereinabove, it is submitted that the combination of Lee et al., Oishi et al., Lee and Hakala would not result in the claimed invention. The combination suggested by the Examiner fails to teach or suggest all the limitations of each claim. The combination of Lee et al., Oishi et al., Lee and Hakala fails to teach a single multiplier, single adder and integration results shift register as taught by the present invention.

The Applicant respectfully traverses the rejection of claims 6-7, 10-13, 16-17, 19, 28, 31 and submits that the presently claimed invention are patently distinct over Lee et al. in view of Oishi et al. and Lee and further in view of Hakala. It is believed that claims 6-7, 10-13, 16-17, 19, 28, 31 overcome the Examiner's § 103(a) rejection based on the Lee et al., Oishi et al., Lee and Hakala references. The Examiner is respectfully requested to withdraw the rejection based on § 103(a).

Regarding claims 26-27:

The Examiner rejected claims 16-17 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,813,262 ("Lee et al.") in view of U.S. Patent No. 6,650,689 ("Oishi et al.") and U.S. Patent No. 6,173,008 ("Lee") and further in view of U.S. Patent No. 6,501,788 ("Wang et al.").

Wang et al. teaches transmitting a symbol in a communications medium according to a first spreading sequence of a set of spreading sequences, for example, CDMA channelization codes, which may be used to transmit symbols in the system. A communications signal is received from the communications medium, for example, at a mobile terminal. The received communications signal is resolved into a plurality of multipath signal components by, for example, descrambling the received signal according to a cell-specific scrambling code. The resolved plurality of signal components is correlated with the set of spreading sequences to generate a respective set of correlations for a respective one of the resolved signal components, a respective one of the sets of correlations including a respective correlation of a resolved signal component with the first spreading sequence.

For the reasons stated hereinabove, it is submitted that the combination of Lee et al., Oishi et al., Lee and Wang et al. would not result in the claimed invention. The combination suggested by the Examiner fails to teach or suggest all the limitations of each claim. The combination of Lee et al., Oishi et al., Lee and Wang et al. fails to teach a single multiplier, single adder and integration results shift register as taught by the present invention.

The Applicant respectfully traverses the rejection of claims 26-27 and submits that the presently claimed invention are patently distinct over Lee et al. in view of Oishi et al. and Lee and further in view of Wang et al. It is believed that claims 26-27 overcome the Examiner's § 103(a) rejection based on the Lee et al., Oishi et al., Lee and Wang et al. references. The Examiner is respectfully requested to withdraw the rejection based on § 103(a).

Regarding claims 26-27, 29, 30, 33-34:

The Examiner rejected claims 26-27, 29, 30, 33-34 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,813,262 ("Lee et al.") in view of U.S. Patent No. 6,650,689 ("Oishi et al."), U.S. Patent No. 6,173,008 ("Lee") and U.S. Patent No. 6,539,048 ("Hakala") and further in view of U.S. Patent No. 6,501,788 ("Wang et al.").

For the reasons stated hereinabove, it is submitted that the combination of Lee et al., Oishi et al., Lee, Hakala and Wang et al. would not result in the claimed invention. The combination suggested by the Examiner fails to teach or suggest all the limitations of each claim. The combination of Lee et al., Oishi et al., Lee, Hakala and Wang et al. fails to teach a single multiplier, single adder and integration results shift register as taught by the present invention.

The Applicant respectfully traverses the rejection of claims 26-27, 29, 30, 33-34 and submits that the presently claimed invention are patently distinct over Lee et al. in view of Oishi et al., Lee and Hakala and further in view of Wang et al. It is believed that claims 26-27, 29, 30, 33-34 overcome the Examiner's § 103(a) rejection based on the Lee et al., Oishi et al., Lee, Hakala and Wang et al. references. The Examiner is respectfully requested to withdraw the rejection based on § 103(a).

Conclusion

In view of the above amendments and remarks, it is respectfully submitted that independent claims 1, 6, 16, 28, 31 and hence dependent claims 2-5, 7-15, 17-27, 29-30, 32-34 are now in condition for allowance. Prompt notice of allowance is respectfully solicited.

In light of the Amendments and the arguments set forth above, Applicant earnestly believes that they are entitled to a letters patent, and respectively solicit the Examiner to expedite prosecution of this patent applications to issuance. Should the Examiner have any questions, the Examiner is encouraged to telephone the undersigned.

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Respectfully submitted,

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